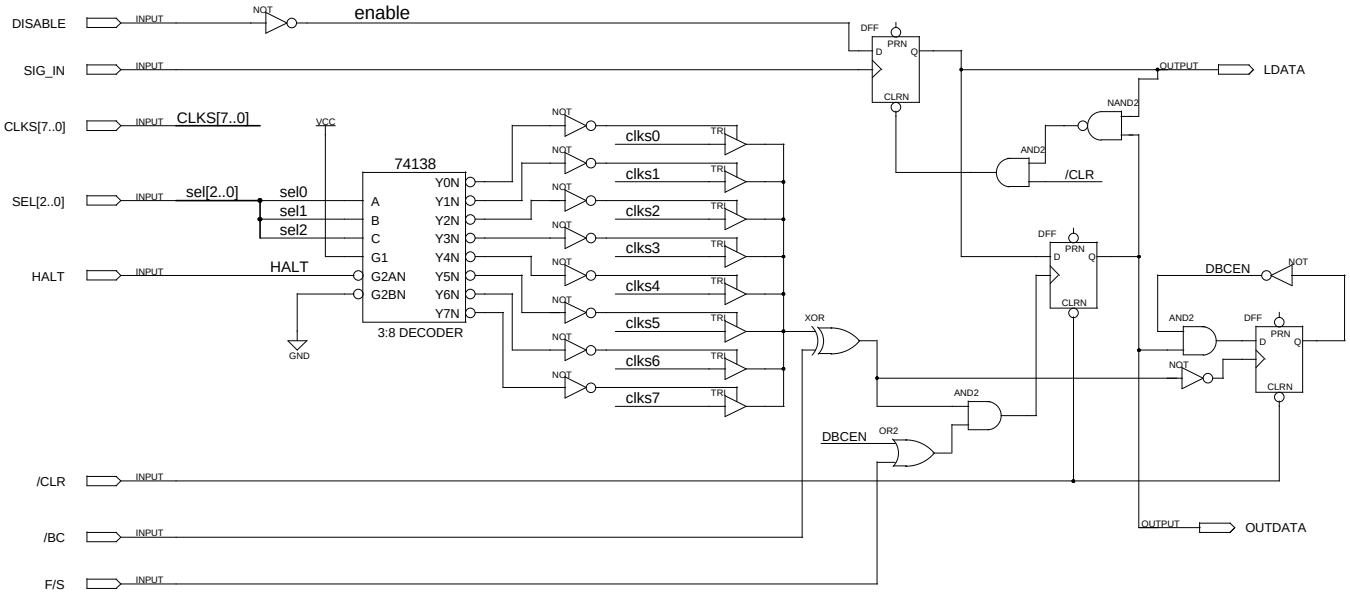
Select the desired skew on the input clocks to delay the input signal when the delayed beam clock arrives. This edge also clears the blocked and the output does not change. the "data" line, however, set of data sent out after the HALT state is removed will not be

The SIG_IN signal is latched asynchronously. This data is clocked out input signal flip-flop. If the HALT line is asserted, the input CLKS are is still enabled and can change during this HALT time. The first good as many of the lines may have gone high.



/BC = 0 Noninverting beam clock
/BC = 1 Inverting beam clock

F/S = 0 Slow gas
F/S = 1 Fast gas

TITLE	8DMUX - Single channel input signal delay		
COMPANY	ORNL		
DESIGNER	Ganesh S. Rao		
SIZE C	NUMBER 1.00	REV A	
DATE 3:12p 9-07-1999	SHEET 1 OF 1		